UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/618,971	07/19/2000	Vikram Gupta	20408-000300US	1379

20350 7590 11/24/2003

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	2

DATE MAILED: 11/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/618,971	GUPTA, VIKRAM	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-43 of the application have been examined.

Drawings

2. The drawings are objected to; see a copy of Form PTO-948 for an explanation.

Claim Objections

3. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

4. Claims 28 and 29 are objected to because of the following informalities:

Claim 28, Lines 1-2, "at least one flip-flops couples to an equal number of said plurality of pads" appears to be incorrect and it appears that it should be "at least one flip-flop couples to an equal number of said plurality of pads".

Claim 29, Lines 1-2, "said at least one flip flops couples to an equal number of said plurality of pads" appears to be incorrect and it appears that it should be "said at least one flip flop couples to an equal number of said plurality of pads".

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 3, 33, 35 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

Claim 3 recites the limitation " said analog circuit portion version affixing step and said analog circuit portion version testing circuit step" in Lines 3-4 of the claim. There is insufficient antecedent basis for these limitations in the claim. Claim 1 refers to "said analog circuit version" and "testing said analog circuit version". It is not clear as to what is meant by "analog circuit portion version testing circuit step", since a testing circuit cannot have a step.

Claim 33 recites the limitation " said analog circuit portion version affixing step and said analog circuit portion version testing circuit step" in Lines 3-4 of the claim. There is insufficient antecedent basis for these limitations in the claim. Claim 31 refers to "said analog circuit version" and "testing said analog circuit version". It is not clear as to what is meant by "analog circuit portion version testing circuit step", since a testing circuit cannot have a step.

Claim 38 recites the limitation " said analog circuit portion version affixing step and said analog circuit portion version testing circuit step" in Lines 3-4 of the claim. There is insufficient antecedent basis for these limitations in the claim. Claim 36 refers to "said analog circuit version" and "testing said analog circuit version". It is not clear as to what is meant by "analog circuit portion version testing circuit step", since a testing circuit cannot have a step.

Claim 35 recites the limitation " said noise generated by said emulation circuit is substantially equivalent to said digital circuit portion " in Lines 1-2 of the claim. This appears to be incorrect since the "noise" cannot be equivalent to "digital circuit portion". It appears it should be " said noise generated by said emulation circuit is substantially equivalent to noise generated by said digital circuit portion ".

Claim Interpretations

7. The following interpretations are used in the art rejections.

In Claim 3, the limitation " said analog circuit portion version affixing step and said analog circuit portion version testing circuit step" are interpreted as "said analog circuit version affixing step and said analog circuit version testing step".

In Claim 33, the limitation " said analog circuit portion version affixing step and said analog circuit portion version testing circuit step" are interpreted as "said analog circuit version affixing step and said analog circuit version testing step".

In Claim 38, the limitation " said analog circuit portion version affixing step and said analog circuit portion version testing circuit step" are interpreted as "said analog circuit version affixing step and said analog circuit version testing step".

In Claim 35, the limitation " said noise generated by said emulation circuit is substantially equivalent to said digital circuit portion " is interpreted as " said noise generated by said emulation circuit is substantially equivalent to noise generated by said digital circuit portion".

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1-7, 19 and 31-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507).

10.1 **IN** teaches microprocessor based mixed signal field programmable integrated device and prototyping methodology. Specifically as per Claim 1, **IN** teaches a method of designing an integrated circuit having digital and analog circuit portions, the digital and analog circuit portions each having defined functions (CL1, L26-32); comprising:

providing an emulation circuit (CL1, L7-11);

affixing the emulation circuit on a test substrate (CL1, L44; CL2, L30-39);

providing a version of the analog circuit portion having at least some of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4);

affixing the analog circuit version on the test substrate (CL1, L63 to CL2, L4); and

testing the analog circuit version (CL2, L4-6; CL1, L36-37; CL2, L30-39).

IN does not expressly teach providing an emulation circuit, which is capable of generating noise. **BO** teaches providing an emulation circuit, which is capable of generating noise (Abstract; CL1, L19-30; CL1, L58-63), as generating and applying noise permits evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included

providing an emulation circuit, which was capable of generating noise, as generating and applying noise would permit evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit.

As per Claim 2, **IN** teaches modifying the analog portion in response to the testing step (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

As per Claim 3, **IN** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion is obtained (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

IN does not expressly teach repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained. **BO** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable

response to the noise effects under operating conditions is obtained (CL1, L50-54), as that would minimize performance degradation of an analog or mixed signal integrated circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

As per Claim 4, **IN** teaches providing a version of the digital circuit portion having all of the defined functions of the digital circuit portion (CL1, L35-36; CL2, L30-39); and

affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4; CL2, L30-39).

IN does not expressly teach affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions. **BO** teaches affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions (CL1, L50-54), as that would minimize performance degradation of an analog or mixed signal

integrated circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

As per Claim 5, **IN** teaches that the digital circuit portion providing step includes testing the defined functions of the digital circuit portion separately from the analog circuit portion (CL1, L32-39; CL2, L30-39).

As per Claim 6, **IN** teaches that the digital circuit portion testing includes programming an FPGA for testing the defined functions of the digital circuit portion (CL1, L41-43; CL1, L63-66).

As per Claim 7, **IN** teaches that the digital circuit portion testing includes simulating the defined functions of the digital circuit portion (CL1, L36; CL2, L30-39).

Per Claim 19: **IN** does not expressly teach that the number of gates in the emulation circuit is substantially equivalent to a number of gates in the digital circuit portion. **BO** teaches that the number of gates in the emulation circuit is substantially equivalent to a number of gates in the digital circuit portion (Abstract, L3-5), as that permits noise to be generated representative

of the digital switching noise generated by the digital integrated circuit (Abstract, L3-5). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included the number of gates in the emulation circuit being substantially equivalent to a number of gates in the digital circuit portion, as that would permit noise to be generated representative of the digital switching noise generated by the digital integrated circuit.

10.2 As per Claim 31, **IN** teaches a method of designing an integrated circuit having digital and analog circuit portions, the digital and analog circuit portions each having defined functions (CL1, L26-32); comprising:

providing an emulation circuit (CL1, L7-11);

affixing the emulation circuit on the integrated circuit (CL1, L44; CL2, L30-39);

providing a version of the analog circuit portion having at least some of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4);

affixing the analog circuit version on the integrated circuit (CL1, L63 to CL2, L4); and

testing the analog circuit version (CL2, L4-6; CL1, L36-37; CL2, L30-39).

IN does not expressly teach providing an emulation circuit, which is capable of generating noise, and which comprises a plurality of logic elements. **BO** teaches providing an emulation circuit, which is capable of generating noise, and which comprises a plurality of logic elements (Abstract; CL1, L19-30; CL1, L58-63), as generating and applying noise permits evaluating any possible performance degradation of an analog or mixed signal integrated circuit

to help determine the need for effective noise suppression techniques and design modification of the circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included providing an emulation circuit, which was capable of generating noise, and which comprised a plurality of logic elements, as generating and applying noise would permit evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit.

As per Claim 32, **IN** teaches modifying the analog portion in response to the testing (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

As per Claim 33, **IN** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion is obtained (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

IN does not expressly teach repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise

effects under operating conditions is obtained. **BO** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained (CL1, L50-54), as that would minimize performance degradation of an analog or mixed signal integrated circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

As per Claim 34, **IN** teaches reconnecting the logic elements to provide for the digital portion (CL2, L30-39).

Per Claim 35: **IN** does not expressly teach that the noise generated by the emulation circuit is substantially equivalent to the digital circuit portion. **BO** teaches that the noise generated by the emulation circuit is substantially equivalent to the digital circuit portion (Abstract, L3-5), as that permits applying the noise for the evaluation of possible degradation of an analog or mixed signal circuit to determine the need for effective noise suppression and

design modifications of the circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** with the method of **BO** that included the number of gates in the emulation circuit being substantially equivalent to a number of gates in the digital circuit portion, as that would permit noise to be generated representative of the digital switching noise generated by the digital integrated circuit.

10.3 As per Claim 36, **IN** teaches an integrated circuit having digital and analog portions (CL1, L26-32); designed by a process comprising:

providing an emulation circuit (CL1, L7-11);

affixing the emulation circuit on a test substrate (CL1, L44; CL2, L30-39);

providing a version of the analog circuit portion having at least some of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4);

affixing the analog circuit version on the test substrate (CL1, L63 to CL2, L4); and

testing the analog circuit version (CL2, L4-6; CL1, L36-37; CL2, L30-39).

IN does not expressly teach providing an emulation circuit, which generates noise. **BO** teaches providing an emulation circuit, which generates noise (Abstract; CL1, L19-30; CL1, L58-63), as generating and applying noise permits evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the design process of **IN** with the design process of **BO** that included providing an

emulation circuit, which generates noise, as generating and applying noise would permit evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit.

As per Claim 37, **IN** teaches modifying the analog portion in response to the testing step (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

As per Claim 38, **IN** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion is obtained (CL2, L11-12; CL2, L16-18; CL1, L63 to CL2, L4; CL2, L30-39; CL4, L37-50).

IN does not expressly teach repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained. **BO** teaches repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable

response to the noise effects under operating conditions is obtained (CL1, L50-54), as that would minimize performance degradation of an analog or mixed signal integrated circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the design process of **IN** with the design process of **BO** that included repeating the affixing emulation circuit step, the analog circuit portion providing step, the analog circuit portion version affixing step and the analog circuit portion version testing circuit step so that a version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions is obtained, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

Per Claim 39: **IN** teaches providing a version of the digital circuit portion having all of the defined functions of the digital circuit portion (CL1, L35-36; CL2, L30-39); and

affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion (CL1, L63 to CL2, L4; CL2, L30-39).

IN does not expressly teach affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions. **BO** teaches affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions

(CL1, L50-54), as that would minimize performance degradation of an analog or mixed signal integrated circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the design process of **IN** with the design process of **BO** that included affixing the digital circuit portion version to an integrated circuit including the version of the analog circuit portion having all of the defined functions of the analog circuit portion, with acceptable response to the noise effects under operating conditions, as that would minimize performance degradation of an analog or mixed signal integrated circuit.

Per Claim 43: **IN** does not expressly teach that the number of gates in the emulation circuit is substantially equivalent to a number of gates in the digital circuit portion. **BO** teaches that the number of gates in the emulation circuit is substantially equivalent to a number of gates in the digital circuit portion (Abstract, L3-5), as that permits noise to be generated representative of the digital switching noise generated by the digital integrated circuit (Abstract, L3-5). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN** with the integrated circuit of **BO** that included the number of gates in the emulation circuit being substantially equivalent to a number of gates in the digital circuit portion, as that would permit noise to be generated representative of the digital switching noise generated by the digital integrated circuit.

11. Claims 8 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), and further in view of **Abiko et al. (AB)** (U.S. Patent 5,193,070).

11.1 As per Claim 8, **IN** and **BO** teach the method of claim 1. **IN** and **BO** do not expressly teach the emulation circuit comprises at least one array comprising at least one shift register. **AB** teaches the emulation circuit comprises at least one array comprising at least one shift register (CL4, L31-38; CL4, L60-67; CL5, 12-14; Cl5, L65 to Cl6, L8; CL6, L8-9), as shift registers permit shifting the contents of the register by specified number of bits (CL6, L8-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** and **BO** with the method of **AB** that included the emulation circuit comprises at least one array comprising at least one shift register, as that would permit shifting the contents of the register by specified number of bits.

11.2 As per Claim 40, **IN** and **BO** teach the integrated circuit of claim 36. **IN** and **BO** do not expressly teach the emulation circuit has at least one array comprising at least one shift register. **AB** teaches the emulation circuit has at least one array comprising at least one shift register (CL4, L31-38; CL4, L60-67; CL5, 12-14; Cl5, L65 to Cl6, L8; CL6, L8-9), as shift registers permit shifting the contents of the register by specified number of bits (CL6, L8-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN** and **BO** with the integrated circuit of **AB** that included the emulation circuit comprises at least one array comprising at least one shift register, as that would permit shifting the contents of the register by specified number of bits.

12. Claims 9-13, 15 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507) and **Abiko et al. (AB)** (U.S. Patent 5,193,070), and further in view of **Porteners et al. (PO)** (U.S. Patent application 2001/0049806).

12.1 As per Claim 9, **IN, BO** and **AB** teach the method of claim 8. **IN, BO** and **AB** do not expressly teach that the testing the analog circuit version is performed while alternately shutting off and turning on at least one array. **PO** teaches that the testing the analog circuit version is performed while alternately shutting off and turning on at least one array (Page 1, Para 2, Para 3, Para 7, Para 8), as that allows the macros to be tested individually for design and test efficiency (Page 1, Para 2, Para 3). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the testing the analog circuit version is performed while alternately shutting off and turning on at least one array, as that would allow the macros to be tested individually for design and test efficiency.

Per Claim 10: **IN, BO** and **AB** do not expressly teach that the shift register comprises a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit. **PO** teaches that the shift register comprises a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit

allow scan chains and seam circuits to be built for circuit testing (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the shift register comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit, as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit would allow scan chains and seam circuits to be built for circuit testing.

IN, BO and **AB** do not expressly teach that the shift register comprises a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern. **PO** teaches that the shift register comprises a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as such plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros (Page 1, Para 5; Page 2, Para 14, Para 23). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the shift register comprising a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern, as such the shift registers comprising

a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit, as such plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern would allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros.

Per Claim 11: **IN, BO, AB** and **PO** teach the method of claim 10. **IN, BO** and **AB** do not expressly teach that the testing the analog circuit version is performed while applying a signal at the clock input. **PO** teaches that the testing the analog circuit version is performed while applying a signal at the clock input (Page 2, Para 14, Para 23; Page 3, Para 25), as that allows the analog and digital circuits to be divided into independent subfunction macros and tested individually using independent clock signals for analog and digital circuits (Page 1, Para 2 and 3; Page 3, Para 25). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the testing the analog circuit version being performed while applying a signal at the clock input, as that would allow the analog and digital circuits to be divided into independent subfunction macros and tested individually using independent clock signals for analog and digital circuits.

Per Claim 12: **IN, BO, AB** and **PO** teach the method of claim 11. **IN, BO** and **AB** do not expressly teach that the testing the analog circuit version is performed while varying the clock input signal. **PO** teaches that the testing the analog circuit version is performed while

varying the clock input signal (Page 2, Para 14, Para 23; Page 3, Para 25), as that allows the data bits to be moved along the flip flops serially from the first clock domain to the second clock domain under the control of the first and second clock signals for testing analog and digital macros (Page 2, Para 14 and 23). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the testing the analog circuit version being performed while varying the clock input signal, as that would allow the data bits to be moved along the flip flops serially from the first clock domain to the second clock domain under the control of the first and second clock signals for testing analog and digital macros.

Per Claim 13: **IN** teaches the testing the analog circuit version is performed while varying the data pattern (CL3, L41-44).

Per Claim 15: **IN, BO, AB** and **PO** teach the method of claim 10. **IN, BO** and **AB** do not expressly teach that the interconnecting blocks comprise a plurality of logic paths, wherein each logic path is comprised of differing amounts of logic gates, and wherein the testing of the analog circuit portion is performed while alternately selecting from among the plurality of logic paths. **PO** teaches that the interconnecting blocks comprise a plurality of logic paths, wherein each logic path is comprised of differing amounts of logic gates, and wherein the testing of the analog circuit portion is performed while alternately selecting from among the plurality of logic paths (Page 1, Para 2, Para 3, Para 7; Page 2, Para 23; Page 3, Para 24 and Para 25), as that allows the analog and digital circuits to be divided into independent subfunction macros and

tested individually (Page 1, Para 2 and 3). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO** and **AB** with the method of **PO** that included the interconnecting blocks comprising a plurality of logic paths, wherein each logic path was comprised of differing amounts of logic gates, and wherein the testing of the analog circuit portion was performed while alternately selecting from among the plurality of logic paths, as that would allow the analog and digital circuits to be divided into independent subfunction macros and tested individually.

Per Claim 41: **IN, BO** and **AB** do not expressly teach that the shift register comprises a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit. **PO** teaches that the shift register comprises a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit allow scan chains and seam circuits to be built for circuit testing (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO** and **AB** with the integrated circuit of **PO** that included the shift register comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit, as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit would allow scan chains and seam circuits to be built for circuit testing.

IN, BO and **AB** do not expressly teach that the shift register comprises a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern. **PO** teaches that the shift register comprises a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as such plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros (Page 1, Para 5; Page 2, Para 14, Para 23). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO** and **AB** with the integrated circuit of **PO** that included the shift register comprising a plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern, as such the shift registers comprising a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit, as such plurality of interconnecting logic blocks, wherein the plurality of flips flops couple to each other through the plurality of interconnecting logic blocks sequentially, and wherein the data bits form a data pattern would allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros.

13. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), **Abiko et al. (AB)** (U.S. Patent 5,193,070), and **Porteners et al. (PO)** (U.S. Patent application 2001/0049806) and further in view of **Ungar (UN)** (U.S. Patent 5,563,524).

13.1 As per Claim 14, **IN, BO, AB** and **PO** teach the method of claim 10. **IN, BO, AB** and **PO** do not expressly teach that the interconnecting logic blocks comprise Exclusive-Or gates, and wherein the testing the analog circuit version is performed while varying the data pattern using the Exclusive-Or gates. **UN** teaches that the interconnecting logic blocks comprise Exclusive-Or gates, and wherein the testing the analog circuit version is performed while varying the data pattern using the Exclusive-Or gates (CL4, L21-32), as that allows the shift register to be configured for different modes of operation and pseudo random signal generation (CL4, L31-32; L22). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO, AB** and **PO** with the method of **UN** that included the interconnecting logic blocks comprising Exclusive-Or gates, and wherein the testing the analog circuit version was performed while varying the data pattern using the Exclusive-Or gates, as that would allow the shift register to be configured for different modes of operation and pseudo random signal generation.

14. Claims 16, 17 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent

5,668,507), **Abiko et al. (AB)** (U.S. Patent 5,193,070), and **Porteners et al. (PO)** (U.S. Patent application 2001/0049806) and further in view of **Lee (LE)** (U.S. Patent RE37,500).

14.1 As per Claim 16, **IN, BO, AB** and **PO** teach the method of claim 10. **IN, BO, AB** and **PO** do not expressly teach that at least one of the flip-flops is coupled to an equal number of pads through an equal number of output drivers, which may be enabled and disabled. **LE** teaches that at least one of the flip-flops is coupled to an equal number of pads through an equal number of output drivers, which may be enabled and disabled (CL2, L66 to CL3, L41; CL5, L9-22; Fig 1), as that allows the mixed analog/digital chip to be divided into analog blocks and digital blocks and using multiplexers connected to the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers (CL1, L52-58). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO, AB** and **PO** with the method of **LE** that included at least one of the flip-flops to be coupled to an equal number of pads through an equal number of output drivers, which may be enabled and disabled, as that would allow the mixed analog/digital chip to be divided into analog blocks and digital blocks and using multiplexers connected to the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers.

Per Claim 17: **IN, BO, AB, PO** and **LE** teach the method of claim 10. **IN, BO, AB** and **PO** do not expressly teach that the testing of the analog circuit portion is performed while

enabling and disabling the output drivers. **LE** teaches that the testing of the analog circuit portion is performed while enabling and disabling the output drivers (CL2, L66 to CL3, L41; CL5, L9-22; Fig 1), as that allows the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers (CL1, L52-58). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN, BO, AB** and **PO** with the method of **LE** that included the testing of the analog circuit portion being performed while enabling and disabling the output drivers, as that would allow the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers.

14.2 As per Claim 20, **IN** teaches an integrated circuit having digital and analog circuit portions (CL1, L26-32).

IN does not expressly teach the digital circuit portion comprising a digital noise emulation circuit. **BO** teaches the digital circuit portion comprising a digital noise emulation circuit (Abstract; CL1, L19-30; CL1, L58-63), as generating and applying noise permits evaluating any possible performance degradation of an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit (CL1, L50-54). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN** with the integrated circuit of **BO** that included the digital circuit portion comprising a digital noise emulation circuit, as generating and applying noise would permit evaluating any possible performance degradation of

an analog or mixed signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit.

IN and **BO** do not expressly teach that the digital noise emulation circuit comprises a control block. **PO** teaches that the digital noise emulation circuit comprises a control block (Page 3, Para 24, Para 26 and Para 31), as the control block allows selecting if the seam circuits should pass data along the normal signal paths or along scan data paths (Page 3, Para 24); and the control signal from the control block can be used to control a latch while shifting data along a scan chain, so the analog macro is not disturbed while scanning data (Page 3, Para 31). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN** and **BO** with the integrated circuit of **PO** that included the digital noise emulation circuit comprising a control block, as the control block would allow selecting if the seam circuits should pass data along the normal signal paths or along scan data paths; and the control signal from the control block could be used to control a latch while shifting data along a scan chain, so the analog macro is not disturbed while scanning data.

IN, BO and **PO** do not expressly teach that the digital noise emulation circuit comprises at least one array, which comprises at least one shift register. **AB** teaches that the digital noise emulation circuit comprises at least one array, which comprises at least one shift register (CL4, L31-38; CL4, L60-67; CL5, 12-14; Cl5, L65 to Cl6, L8; CL6, L8-9), as shift registers permit shifting the contents of the register by specified number of bits (CL6, L8-9). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO** and **PO** with the integrated circuit of **AB** that included that the

digital noise emulation circuit comprising at least one array, which comprised at least one shift register, as that would permit shifting the contents of the register by specified number of bits.

IN, BO, AB and **PO** do not expressly teach that the digital noise emulation circuit comprises a plurality of pads. **LE** teaches that the digital noise emulation circuit comprises a plurality of pads (CL2, L66 to CL3, L41; CL5, L9-22; Fig 1), as that allows the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers (CL1, L52-58). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB** and **PO** with the integrated circuit of **LE** that included the digital noise emulation circuit comprising a plurality of pads, as that would allow the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers.

Per Claim 21: **IN, BO, AB** and **LE** do not expressly teach that each array comprises a plurality of flip-flops coupled to each other through interconnecting logic blocks. **PO** teaches that each array comprises a plurality of flip-flops coupled to each other through interconnecting logic blocks (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as arrays comprising a plurality of flip-flops coupled to each other through interconnecting logic blocks allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros (Page 1, Para 5; Page 2, Para 14, Para 23). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB** and **LE** with the integrated circuit of **PO** that included each array comprising a

plurality of flip-flops coupled to each other through interconnecting logic blocks, as arrays comprising a plurality of flip-flops coupled to each other through interconnecting logic blocks would allow scan chains and seam circuits to be built for mixed signal testing in circuits involving analog and digital macros.

Per Claim 22: **IN, BO, AB** and **LE** do not expressly teach that the flip-flops and interconnecting logic blocks are coupled sequentially. **PO** teaches that the flip-flops and interconnecting logic blocks are coupled sequentially (Page 1, Para 5; Page 2, Para 14, Para 23; Figs 3 and 4), as the flip-flops and interconnecting logic blocks coupled sequentially allow serially moving a data bit along its flip flops from the first to the second clock domain for testing mixed signal IC with analog and digital blocks (Page 2, Para 14, Para 23). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB** and **LE** with the integrated circuit of **PO** that included the flip-flops and interconnecting logic blocks are coupled sequentially, as the flip-flops and interconnecting logic blocks coupled sequentially would allow serially moving a data bit along its flip flops from the first to the second clock domain for testing mixed signal IC with analog and digital blocks.

15. Claims 18 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), and further in view of **Perkins et al. (PE)** (U.S. Patent 6,625,557).

15.1 As per Claim 18, **IN** and **BO** teach the method of claim 1. **IN** and **BO** do not expressly teach that the analog circuit portion includes an RF circuit subportion. **PE** teaches that the analog circuit portion includes an RF circuit subportion (CL1, L52-54; CL6, L1-32), as that allows testing analog circuits with radio frequency signals (CL6, L1-32). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **IN** and **BO** with the method of **PE** that included the analog circuit portion including an RF circuit subportion, as that would allow testing analog circuits with radio frequency signals.

15.2 As per Claim 42, **IN** and **BO** teach the integrated circuit of claim 36. **IN** and **BO** do not expressly teach that the analog circuit portion includes an RF circuit subportion. **PE** teaches that the analog circuit portion includes an RF circuit subportion (CL1, L52-54; CL6, L1-32), as that allows testing analog circuits with radio frequency signals (CL6, L1-32). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN** and **BO** with the integrated circuit of **PE** that included the analog circuit portion including an RF circuit subportion, as that would allow testing analog circuits with radio frequency signals.

16. Claims 23-25, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), **Abiko et al. (AB)** (U.S. Patent 5,193,070) **Porteners et al. (PO)** (U.S. Patent

application 2001/0049806) and **Lee (LE)** (U.S. Patent RE37,500), and further in view of **Davis et al. (DA)** (U.S. Patent 5,754,764).

16.1 As per Claim 23, **IN, BO, AB, PO** and **LE** teach the integrated circuit of claim 22. **IN, BO, AB, PO** and **LE** do not expressly teach that the control block comprises a plurality of configuration registers, at least one input line and a decoder block for selecting one of the configuration registers for updating from the at least one input line. **DA** teaches that the control block comprises a plurality of configuration registers, at least one input line and a decoder block for selecting one of the configuration registers for updating from the at least one input line (Fig 1A; Figs. 2A, 2B; CL5, L62 to CL6, L7; CL4, L66 to CL5, L6; Fig 1), as the configuration registers control enabling and disabling of the functions, assignment of the registers, mode selection and power down (CL4, L67 to CL5, L2); the input permits the chip options to be configured by software (Cl5, L6); and the address decoder provides selection of addresses of various blocks in the circuit (CL6, L2-4). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB, PO** and **LE** with the integrated circuit of **DA** that included the control block comprising a plurality of configuration registers, at least one input line and a decoder block for selecting one of the configuration registers for updating from the at least one input line, as the configuration registers would control enabling and disabling of the functions, assignment of the registers, mode selection and power down; the input would permit the chip options to be configured by software; and the address decoder would provide selection of addresses of various blocks in the circuit.

Per Claim 24: **IN, BO, AB, PO, LE** and **DA** teach the integrated circuit of claim 23. **IN, BO, AB, LE** and **DA** do not expressly teach that the interconnecting blocks comprise a plurality of logic paths, each path comprising a different amount of logic gates. **PO** teaches that the interconnecting blocks comprise a plurality of logic paths, each path comprising a different amount of logic gates (Page 1, Para 2, Para 3, Para 7; Page 2, Para 23; Page 3, Para 24 and Para 25), as that allows the analog and digital circuits to be divided into independent subfunction macros and tested individually (Page 1, Para 2 and 3). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB, LE** and **DA** with the integrated circuit of **PO** that included the interconnecting blocks comprising a plurality of logic paths, each path comprising a different amount of logic gates, as that would allow the analog and digital circuits to be divided into independent subfunction macros and tested individually.

Per Claim 25: **IN, BO, AB, PO** and **LE** do not expressly teach that the plurality of logic paths are under control of one of the configuration registers. **DA** teaches that the plurality of logic paths are under control of one of the configuration registers (Figs. 2A, 2B; CL11, L31 to CL12, L4), because as per **PO** that permits different circuit blocks to be selected and tested individually for improving design and test efficiency (Page 1, Para 2 and 3), selecting the circuit blocks by configuring the configuration registers through software control (**DA**: CL5, L6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB, PO** and **LE** with the integrated circuit of **DA** that

included the plurality of logic paths being under control of one of the configuration registers, as that permits different circuit blocks to be selected and tested individually for improving design and test efficiency, selecting the circuit blocks by configuring the configuration registers through software control.

Per Claim 28: **IN, BO, AB, PO, LE** and **DA** teach the integrated circuit of claim 23. **IN, BO, AB, PO** and **DA** do not expressly teach that at least one flip-flops couples to an equal number of the plurality of pads. **LE** teaches that at least one flip-flops couples to an equal number of the plurality of pads (CL2, L66 to CL3, L41; CL5, L9-22; Fig 1), as that allows the mixed analog/digital chip to be divided into analog blocks and digital blocks and using multiplexers connected to the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers (CL1, L52-58). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB, PO** and **DA** with the integrated circuit of **LE** that included at least one flip-flops coupling to an equal number of the plurality of pads, as that would allow the mixed analog/digital chip to be divided into analog blocks and digital blocks and using multiplexers connected to the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers.

Per Claim 29: **IN, BO, AB, PO, LE** and **DA** teach the integrated circuit of claim 28. **IN, BO, AB, PO** and **DA** do not expressly teach that the at least one flip flops couples to an equal

number of the plurality of pads though an equal number of output drivers. **LE** teaches that the at least one flip flops couples to an equal number of the plurality of pads though an equal number of output drivers (CL2, L66 to CL3, L41; CL5, L9-22; Fig 1), as that allows the mixed analog/digital chip to be divided into analog blocks and digital blocks and using multiplexers connected to the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers (CL1, L52-58). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB, PO** and **DA** with the integrated circuit of **LE** that included the at least one flip flops coupling to an equal number of the plurality of pads though an equal number of output drivers, as that would allow the mixed analog/digital chip to be divided into analog blocks and digital blocks and using multiplexers connected to the internal ports between blocks the internal ports to be either controlled or observed from external I/O pads, depending on the test mode of the control signals applied to the multiplexers.

17. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), **Abiko et al. (AB)** (U.S. Patent 5,193,070) **Porteners et al. (PO)** (U.S. Patent application 2001/0049806) and **Lee (LE)** (U.S. Patent RE37,500), and further in view of **Davis et al. (DA)** (U.S. Patent 5,754,764) and **Ungar (UN)** (U.S. Patent 5,563,524).

17.1 As per Claim 26, **IN, BO, AB, PO, LE** and **DA** teach the integrated circuit of claim 23. **IN, BO, AB, PO, LE** and **DA** do not expressly teach that the interconnecting logic blocks comprise Exclusive-Or gate. **UN** teaches that the interconnecting logic blocks comprise Exclusive-Or gates (CL4, L21-32), as that allows the shift register to be configured for different modes of operation and pseudo random signal generation (CL4, L31-32; L22). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB, PO, LE** and **DA** with the integrated circuit of **UN** that included the interconnecting logic blocks comprising Exclusive-Or gate, as that would allow the shift register to be configured for different modes of operation and pseudo random signal generation.

18. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), **Abiko et al. (AB)** (U.S. Patent 5,193,070), **Porteners et al. (PO)** (U.S. Patent application 2001/0049806), **Lee (LE)** (U.S. Patent RE37,500) and **Davis et al. (DA)** (U.S. Patent 5,754,764), and further in view of **Ungar (UN)** (U.S. Patent 5,563,524) and **Dummermuth et al. (DU)** (U.S. Patent 4,831,510).

18.1 As per Claim 27, **IN, BO, AB, PO, LE, DA** and **UN** teach the integrated circuit of claim 26. **IN, BO, AB, PO, LE, DA** and **UN** do not expressly teach that the exclusive-or gates receive at least one input from one of the configuration registers. **DU** teaches that the exclusive-or gates receive at least one input from one of the configuration registers (CL9, L24-42), as that allows

the other input to the exclusive OR gate to be inverted before being processed by supplying an input to the exclusive OR gate from the configuration register (CL9, L31-33). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB, PO, LE, DA** and **UN** with the integrated circuit of **DU** that included the exclusive-or gates receiving at least one input from one of the configuration registers, as that would allow the other input to the exclusive OR gate to be inverted before being processed by supplying an input to the exclusive OR gate from the configuration register.

19. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Insenser Farre. (IN)** (U.S. Patent 6,460,172) in view of **Boerstler et al. (BO)** (U.S. Patent 5,668,507), **Abiko et al. (AB)** (U.S. Patent 5,193,070), **Porteners et al. (PO)** (U.S. Patent application 2001/0049806), **Lee (LE)** (U.S. Patent RE37,500) and **Davis et al. (DA)** (U.S. Patent 5,754,764), and further in view of **Dummermuth et al. (DU)** (U.S. Patent 4,831,510).

19.1 As per Claim 30, **IN, BO, AB, PO, LE** and **DA** teach the integrated circuit of claim 29. **IN, BO, AB, PO, LE** and **DA** do not expressly teach that the output drivers may be enabled and disabled by one of the configuration registers. **DU** teaches that the output drivers may be enabled and disabled by one of the configuration registers (CL9, L45-48), because as per **DA** that allows enabling and disabling various logic blocks by setting the configuration register (CL4, L67 to CL5, L2). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the integrated circuit of **IN, BO, AB, PO, LE** and **DA** with the integrated circuit of **DU** that included the output drivers being enabled and disabled by one of

the configuration registers, as that would allow enabling and disabling various logic blocks by setting the configuration register.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
November 13, 2003

HUGH JONES PH.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100